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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/256,265	02/23/1999	DAH-BIN KAO	16405-311	9612

7590 12/17/2003

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/256,265	KAO ET AL.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,8-10,16,17 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2 and 8-10* is/are allowed.

6)☒ Claim(s) *16,17 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 16 and 23-24 are still rejected under 35 U.S.C. 102(b) as being anticipated by Eitan et al. (US Patent No. 4,998,220).

Regarding claim 16, Eitan et al. teaches a semiconductor device comprising: a substrate (103) having channel region (140, 142) defined thereon (see Figs. 6 and 7b); a first insulating layer disposed over said channel region and over at least a portion of said substrate (consider portion of the layer 105a, which is between the floating gate 104a and the channel region 140, 142) (see Figs. 6, 7a and 7b); a floating gate (104a) having at least a substantial portion thereof disposed over said channel region (140, 142) and separated therefrom by said first insulating layer (see Figs. 6 and 7b), said floating gate (104a) having at least two side walls and a top surface (see Figs. 6, 7a, 7b and 7e); a second insulating layer disposed over said sidewalls and over said top surface of said floating gate (consider portion of the layer 105a, which is over the floating gate 104a and between the control gate 106 and the erase gate 108) (see Figs. 6, 7a, 7b and 7e); a control gate (106) having a first portion disposed over a portion of said channel region (140, 142) and being separated therefrom by said second insulating layer (see Figs. 6, 7A and 7b), a second portion formed over a first one of said side

walls and a third portion over at least a first portion of said top surface of said floating gate and being separated from said floating gate by said second insulating layer (see Figs. 6, 7A and 7b), said second portion having a surface substantially parallel to and opposing said first side wall (see Figs. 6, 7A and 7b); an erase gate (108) formed over a second one of said side walls (see Figs. 6, 7a and 7e) and over at least a second portion of said top surface of said floating gate and being separated from said second one of said side walls and said portion of said top surface of said floating gate by said second insulating layer (see Figs. 6, 7a and 7e); a drain region (102a) formed in a portion of said substrate proximate said control gate (see Figs. 6, 7a and 7b); and a source region (110) formed in a portion of said substrate proximate said erase gate (see Figs. 6, 7a and 7e). With regards to the limitation *whereby/wherein* "during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process", Applicant should note that it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2USPQ F.2d 1647 (1987). However, even if such limitation is considered, Eitan et al. still anticipates the claimed limitation by disclosing the required functional erasing/programming operation in which source and control gate are held at 0 volts, and the erase gate is held at a high voltage (see col. 13, lines 25-31).

Regarding claim 23, Eitan et al. teaches a memory array comprising: a substrate (103) having a channel region (140, 142) (see Figs. 5, 6 and 7b, and Abstract); a first insulating layer (consider portion of the layer 105a, which is between the floating gate 104a and the channel region 140, 142) (see Figs. 6, 7a and 7b); a floating gate (104a), a second insulating layer (consider portion of the layer 105a, which is on top of the floating gate 104a and between the control gate 106 and the erase gate 108) (see Figs. 6, 7a and 7b); a control gate (106) having a portion disposed over a portion of said channel region (140, 142) and being separated therefrom by said second insulating layer (see Figs. 6 and 7b), and wherein a portion of said control gate is disposed in facing relationship to a side surface of said floating gate and is separated from said floating gate by said second insulating layer (see Figs. 6, 7a and 7b), an erase gate (108) formed over one of the sides of said floating gate (104a) and being separated by said second insulating layer (see Figs. 6 and 7a), a drain region (102a), a source region (110), (see Figs. 5, 6, 7a and 7b, and Abstract); a plurality of rows and columns (see Fig. 5) of interconnected memory cells wherein the control gates are connected by a common word line (106) (see Fig. 5), the erase gates are connected by a common erase line (108) (see Fig. 5), the source regions are connected by a common source line (110) (see Fig. 5), and the drain regions are connected by a common drain line (139) (see Fig. 7b and col. 6, lines 55-58); and a source region (110) formed in a portion of said substrate proximate said erase gate (see Figs. 6, 7a and 7e). With regards to the limitation *whereby/wherein* "during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential

applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process", Applicant should note that it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2USPQ F.2d 1647 (1987). However, even if such limitation is considered, Eitan et al. still anticipates the claimed limitation by disclosing the required functional erasing/programming operation in which source and control gate are held at 0 volts, and the erase gate is held at a high voltage (see col. 13, lines 25-31).

Regarding claim 24, Eitan et al. further teaches that the floating gate (104a) has at least a substantial portion thereof disposed over the channel region (140, 142) (see Figs. 6 and 7b) and is separated therefrom by said first insulating layer (consider portion of the layer 105a, which is between the floating gate 104a and the channel region 140, 142) (see Figs. 6 and 7b), said control gate (106) is substantially placed on one side of said floating gate (104a) (see Figs. 6, 7a and 7b) and separated therefrom by said second insulation layer (consider portion of the layer 105a, which is over the floating gate 104a, and between the control gate 106 and the erase gate 108) (see Figs. 6, 7a and 7b), said erase gate (108) is substantially placed on a second side of said floating gate (104a) (see Figs. 6, 7a and 7e) and is separated therefrom by said second insulation layer (consider portion of the layer 105a, which is over the floating gate 104a, and between the control gate 106 and the erase gate 108) (see Fig. 6, 7a, 7b and 7e), said drain region (102a) is substantially disposed on said side of said floating gate, and

said source region (110) is substantially disposed on said second side of said floating gate (see Figs. 6, 7a and 7b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 17 and 25 are still rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan et al. (US Patent No. 4,998,220) in view of Chang (US Patent No. 6,125,060).

Regarding claims 17 and 25, Eitan et al. teaches an erase gate (108) overlapping the floating gate (104a) (see Fig. 6 and 7e). However, Eitan et al. fails to teach an erase gate overlapping a portion of the control gate. Chang teaches that is well known in the

art to extend the erase gate (122) to cover portions of the control gate (101) and the floating gate (103) (see Fig. 1F). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Eitan et al. to include an erase gate that overlaps portions of the floating gate and the control gate. The ordinary artisan would have been motivated to modify Eitan et al. in the manner described above for at least the purpose of achieving high speed programming with low power consumption.

Allowable Subject Matter

6. Claims 1-2 and 8-10 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a semiconductor device comprising a control gate disposed over a portion of a channel region, a first one of the sidewalls of a floating gate, and a first portion of a top surface of the floating gate; an erase gate disposed over a second one of the sidewalls of the floating gate, and a second portion of the top surface of the floating gate; a drain region formed proximate to the portion of the control gate disposed over the channel region; and a source region formed proximate said erase gate and having a substantial portion thereof underneath said floating gate.

Response to Arguments

8. With regards to claims 16-17 and 23-25, Applicant's arguments filed September 26, 2003 have been fully considered but they are not persuasive. Applicant argued that the reference Eitan et al. fails to teaches a drain region formed in a portion of the substrate which is proximate the portion of the control gate which is disposed over the channel region and is separated from the channel region by the second insulating layer (see page 8 of the REMARKS). However, Applicant has overlooked the express teaching of Eitan et al. For example, Eitan et al teaches:

a) a control gate (106) disposed:

i. over a first portion of a top surface of the floating gate (104a) (see figure 7a, which is a cross sectional view along the line A-A in figure 6),

ii. over a first one of the sidewalls of a floating gate (106) (see figure 7a)

iii. over a portion of a channel region (140) (see figure 7b, which is the cross sectional view along the line B-B in figure 6. Please note that figure 7b shows a further portion of the control gate not shown in figure 7a).

iv. a second insulating layer between the control gate (106) and the floating gate (104a) (consider the space between the control gate and the floating gate in figures 7a and 7b as the second insulating layer).

b) a drain region (102a) **proximate** to the control gate (106) (see figures 6 and 7b).

Therefore, applicant's arguments are not persuasive since Eitan et al. teaches the claimed limitation of a drain region proximate to the control gate.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078 or (571) 272-1727, after February 9, 2004. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD

Tom Thomas